

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An interface circuit for processing an ~~analog color~~ input signal comprising:

a phase locked loop (PLL) circuit adapted to generate a plurality of phased signals from a synchronizing signal that is associated with the ~~analog color~~ input signal, wherein the PLL is arranged to provide each phased signal of the plurality of phased signals on at least one corresponding separate signal line of a plurality of signal lines;

a phase adjuster including:

a first phase selector for selecting a first one of the phased signals;

a second phase selector for selecting a second one of the phased signals; and

a phase mixer for multiplying the first selected phased signal with a first weight,

multiplying the second selected phased signal with a second weight, and adding together

the first and the second multiplied phased signals to derive the adjustable delay signal, wherein the first selected phased signal, the second selected phased signal, and at least one selected phase

information signal are received into the phase mixer adapted to generate an adjustable delay signal

from two of the plurality of phased signals that are apart from each other by an odd multiple of approximately 45 degrees; and

~~an analog to digital converter adapted to improve processing of the analog color signal by choosing an adjustment to the delay signal, wherein at least one simulated phase signal is provided.~~

2. (Original) The circuit of claim 1, wherein
the synchronizing signal is intended to generate a pixel clock in a display, and
the phased signals replicate those of the pixel clock.

3. (Canceled)

4. (Currently Amended) The circuit of claim [[3]]1, wherein
the phase adjuster further includes:
a decoder to generate phase selection signals for selecting the first and second phased signals.

a phase adjuster adapted to generate an adjustable delay signal from two of the plurality of phased signals that are apart from each other by an odd multiple of approximately 45 degrees, wherein the phase adjuster includes:

a phase mixer for multiplying the first selected phased signal with a first weight,

a decoder to generate phase selection signals for selecting the first and second phased signals; and

6. (Currently Amended) The circuit of claim [[3]]1, wherein the phase adjuster further includes:

wherein the phase mixer receives the first weight signal and the second weight signal to derive the adjustable delay signal.

7. (Original) The circuit of claim 6, wherein the phase adjuster further includes:

a decoder to generate weight selection signals for generating the first and second weight signals.

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means for choosing an adjustment to the adjustable delay signal ~~to improve conversion of the color signal into digital form~~, wherein at least one simulated phase signal is provided.

12. (Original) The device of claim 11, wherein

the means for deriving the phased signals includes phase locked loop (PLL) circuit.

13. (Currently Amended) A method for generating a delay signal for processing an ~~analog color~~ input signal, comprising:

deriving a plurality of phased signals from a synchronizing signal associated with the ~~analog color~~ input signal, wherein the PLL is arranged to provide each phased signal of the plurality of phased signals on at least one corresponding separate signal line of a plurality of signal lines;

deriving the delay signal from two of the plurality of phased signals including: that are apart from each other by an odd multiple of approximately 45 degrees, wherein a delay generated by the delay signal is adjustable

selecting two phased signals from the plurality of phased signals;

providing at least one selected phase information signal;

multiplying a first one of the selected phased signals with a first weight, wherein the first weight is based, at least in part, on the at least one selected phase information signal;

multiplying a second one of the selected phased signals with a second weight, wherein the second weight is based, at least in part, on the at least one selected phase information signal; and

adding together the first and the second multiplied phased signals; and

choosing an adjustment to the delay signal to improve conversion of the ~~analog color~~ input signal into digital form, wherein at least one simulated phase signal is provided.

14. (Original) The method of claim 13, wherein

the phased signals are derived in a phase locked loop (PLL) circuit.

15. (Previously Presented) The method of claim 14, wherein

the synchronizing signal is intended to generate a pixel clock in a display, and

the phased signals replicate those of the pixel clock.

16. (Currently Amended) The method of claim 13, wherein deriving is performed by:
determining the location of a general requested delay in a phase diagram;~~and~~
selecting, wherein the two phased signals are selected such that they define a sector between on the phase diagram that encompasses the general required delay.
17. (Canceled)
18. (Currently Amended) The method of claim ~~[[17]]~~13, further comprising:
selecting first and second weights so as to simulate the general requested delay within the sector.
19. (Original) The method of claim 18, further comprising:
subtracting the first weight from a preset sum total weight to derive the second weight.
20. (Original) The method of claim 19, wherein
the sum total weight equals a multiplication integer times four, and
the first weight equals the multiplication integer times one of zero, one, two,
three and four.
- 21-26. (Not Entered)
27. (Currently Amended) An interface ~~[[The]] circuit of claim 5 for processing an input signal,~~
comprising:
a phase locked loop (PLL) circuit adapted to generate a plurality of phased signals from a
synchronizing signal that is associated with the input signal;
a phase adjuster adapted to generate an adjustable delay signal from two of the plurality of
phased signals, wherein the phase adjuster includes:
a phase mixer, including:
at least three differential pairs, wherein a first one of the differential pairs is

arranged to multiply a ~~[[the]]~~ first selected phased signal with a ~~[[the]]~~ first weight and a second one of the differential pairs is arranged to multiply a ~~[[the]]~~ second selected phased signal with a ~~[[the]]~~ second weight, and wherein the phase mixer is configured to activate two differential pairs from the at least three differential pairs to derive the adjustable delay signal, ~~based, in part, on the at least one selected phase information signal; and~~

28. (Previously presented) The circuit of claim 27, wherein the more than two differential pairs includes at least four differential pairs.

29. (Previously presented) The circuit of claim 28, wherein the phase mixer is arranged such that the selection of active differential pairs sets the polarity of the adjustable delay signal.

30. (Currently Amended) The circuit of claim ~~[[5]]~~1, wherein the phase mixer includes:
a first switch coupled between a first node and a second node, wherein the first switch is arranged to receive the first weight signal at the first node;
a first differential pair having at least a first input, a second input, and an output, wherein the first differential pair is arranged to receive the first selected phased signal at the first input, and wherein the second input is connected to the second node;
a second switch coupled between a third node and a fourth node, wherein the second switch is arranged to receive the first weight signal at the third node;
a second differential pair having at least a first input, a second input, and an output, wherein the second differential pair is arranged to receive the first selected phased signal at the first input, and wherein the second input is connected to the fourth node;
a third switch coupled between a fifth node and a sixth node, wherein the third switch is arranged to receive the first weight signal at the fifth node; and
a third differential pair having at least a first input, a second input, and an output, wherein the third differential pair is arranged to receive the second selected phased signal at the first input, and wherein the second input is connected to the sixth node.

31. (Previously presented) The circuit of claim 30, wherein the phase mixer further includes:

a fourth differential pair having at least a first input, a second input, and an output, wherein the fourth differential pair is arranged to receive the second selected phased signal at the first input, and wherein the second input is connected to the eighth node, wherein the outputs of the differential pairs are connected to an output bus.

33. (New) The circuit of claim 1, further comprising:

34. (New) An interface circuit for processing an input signal comprising:

a phase adjuster including:

a Phase Digital to Analog Converter, including:

a second current source circuit that is arranged to receive a second control input, wherein while the second control input is at a first logic level, the second current source circuit provides

a phase mixer for multiplying a first selected phased signal with the first weight, multiplying a second selected phased signal with the second weight, and adding together the first and the second multiplied phased signals to derive the adjustable delay signal.

36. (New) The circuit of Claim 34, wherein the first current source circuit includes:

wherein the second current source circuit includes:

a second transistor that is arranged to couple the first transistor to the first weight signal while the second control signal is asserted; and

a third transistor that is arranged to couple the first transistor to the second weight signal while the third control signal is deasserted.

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